ABSTRACT OF THE DISCLOSURE

In a structure in which a plurality of signals related to each other are supplied to a driving circuit in such a manner that at least one of the signals is supplied also to the other circuit, the present invention prevents change of phase relation between the plural signals due to difference in wiring load, without directly processing the signals with higher power consumption. The first and second clock signals SCK1 and SCK2 are supplied to the first data signal line driving circuit SD1, while the first clock signal SCK1 is also supplied to the second data signal line driving circuit SD2 in parallel. The wirings 1 and 2 for the respective signals are adjusted to have equal wiring load with a dummy wiring 2 provided in the wiring 2, for solving uneven wiring load caused by difference of leading manner, the dummy wiring 2 constituting an additional capacitor section 7, together with a liquid crystal layer and a counter electrode.